REMARKS

Claims 32-83 are pending in this continuation application. Claims 33, 37, 41 and 46 have been cancelled by amendment. In the Office Action dated August 7, 2006, the Examiner took the following action: (1) rejected claims 32-35, 37-44, 46-56, 58-66 and 68-83 under 35 U.S.C. § 102(b) as being anticipated by Intel MultiProcessor Specification ("Intel"); (2) rejected claims 32, 40, 50, 60, 70 and 76 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,884,091 to Ghori et al. ("Ghori"); and (3) rejected claims 36, 45, 57 and 67 under 35 U.S.C. § 103(a) as being unpatentable over Intel in view of Official Notice.

In accordance with the Examiner's request, the Applicants are submitting a copy of pages 5-10 of the "Open VMS DCL Dictionary" reference. Applicants would like to bring to the Examiner's attention that this reference was originally cited in the parent application by Examiner Samuel Broda. He specifically cited pages 5-10. Also enclosed for the Examiner's review is a copy of the original form PTO-892 in which Examiner Broda cites the reference.

As to the rejections which encompass claims 32-35, 37-44, 46-56, 58-66 and 68-83 under 35 U.S.C. § 102(b) and Intel, Applicants disagree with the Examiner's grounds of rejection under 35 U.S.C. § 102(b). With regard to claims 32, 40, 50, 60, 70 and 76 that were rejected under 35 U.S.C. § 102(b), Applicants have amended these claims by adding a limitation from claims that depend from each respectively, and cancelled or amended such dependent claims.

The disclosed embodiments of the invention will now be discussed in comparison to this prior art to clarify various distinctions of Applicants' invention over the cited art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

An embodiment of the disclosed method selects a compatible processor for addition to a multiprocessor computer by using processor compatibility information. The multiprocessor computer has at least one current processor in a slot or socket and at least one additional slot or socket in which a new processor can be added. Each processor is a associated

with a number that identifies that particular processor. The method executes a software program on a computer to determine the number of processors in the multiprocessor computer and the identification numbers of each of these. The method then obtains compatibility information from a remote location. And finally, the method executes a software program that compare the identification numbers of the processors with the processor compatibility information to determine which, if any, other processors are compatible with the current processors.

The Intel reference is a specification for an enhanced PC manufacturing standard for DOS-compatible systems. The specification is intended to provide a multiprocessor computing interface standard that allows for the extension of the PC/AT platform to a multiprocessor realm while still maintaining binary compatibility with legacy single processor platforms. The specification contemplates that a multiprocessor computer will be comprised of one bootstrap processor ("BSP") and one or more application processors ("AP"). At boot time, the bootstrap processor will have sole control of the system and its busses and only at a later time will any of the AP's be allowed to start. See pg. 4-3. At the heart of the specification are data structures that define the configuration of a multiprocessor system. These data structures are the "MP Configuration Table" and "Floating Point Structure." See Figure 4-1, pg. 4-1. The Floating Point Structure is a data structure containing a physical address pointer to the MP Configuration Table and is located in one of three possible locations in system memory. The Floating Point Structure must be present in system memory to indicate that the system conforms to the MultiProcessor Specification. See pg. 4-2. The information in these data structures is used by the operating system for, among other things, starting the AP's.

The MP Configuration Table is a configurable and optional data structure used to store information about the multiprocessor configuration including information about advanced programmable interrupt controllers, processors, buses and interrupts. It is important to note that the MP Configuration Table is a data structure. That is, the MP Configuration Table is, by definition, a structure in memory for storing information. The MP Configuration Table cannot be a computer implemented method, or software and it is not executable code of any kind.

Although the possible memory locations of the Floating Point Structure are rigidly specified, the location of the MP Configuration Table data structure is not strictly controlled. The specification does, however, recommend specific locations for the table.

Although the Examiner contends that one of these recommended locations, "(b) Within the last kilobyte of system base memory" can be a "remote computer," it is clear from context that "system base memory" is part of system memory and not part of any remote computer. This is true at least because, for some configurations, the system BIOS is responsible for building the MP Configuration Table data structure. See pg. A-1. The system BIOS does not have access to a "remote computer" and therefore the MP Configuration Table data structure could not be built in such a location. This is made further clear on page A-5: "The table can be located within any unreported, hidden system memory space or with the BIOS ROM region."

For the reasons discussed above, the Intel reference fails to disclose a method of selecting a compatible processor for addition to a multiprocessor computer. In fact, the Intel reference does not and cannot disclose such a method because it is only specifies the form and content of the Floating Point Structure and the MP Configuration Table data structures.

Ghori discloses an upgrade central processing unit ("CPU") that includes handshake circuitry enabling such an upgrade CPU to communicate information about itself with the original CPU in the computer system. Upon system power-up or upon a reset, the original system CPU determines if there is a CPU in the upgrade socket and if so, what kind of CPU is present. The information about the upgrade CPU's identification and cooperative relationship capability is stored in either a discrete memory device incorporated into the interprocessor circuitry or burned directly into the read-only memory of the processor. See col. 4, lines 53-61. This information is used by the original system CPU to configure the system. Although not claimed, Ghori also discloses that such information might be used by the operating system to further customize system operation.

Turning, now, to the claims, Intel fails to disclose each and every limitation of amended claims 32 and 40. Amended claims 32 and 40 are directed towards a method of selecting a compatible processor for addition to a multiprocessor computer. In particular, the method requires "executing a computer program comparing the identifying information for each current processor in the multiprocessor computer with the accessed processor compatibility information to determine the processors that are compatible with each current processor." Intel fails to disclose executing a computer program that compares such information. As was discussed above, Intel discloses data structures that are required for compliance with the

MultiProcessor specification and does not teach a method of selecting a compatible processor because it does not teach or fairly suggest executing such a program.

Moreover, amended claims 32 and 40 require that the accessed processor compatibility information be located on, and retrieved from, a computer that is remote from the multiprocessor computer. As was discussed above, Intel discloses certain data structures. It does not teach or suggest a method for accessing these data structures or retrieving the information therein. Even if Intel does suggest a method for accessing these data structures, it is clear that these data structures exist only on the computer system and not on a computer that is remote from the multiprocessor computer. For these reasons, amended claims 32 and 40 are not anticipated by Intel.

Amended claims 50 and 60 are directed towards a system for selecting a new processor for addition to a multiprocessor computer. Both claims require a "component remote from the multiprocessor computer that store processor compatibility information." Intel does not teach or suggest storing "compatibility information." Intel does teach storing certain types of information about processors, but it does not suggest or teach that this information is necessarily related to "compatibility." Even if it does suggest or teach storing "compatibility information," it does not disclose storing such information in a remote component. Instead, Intel discloses certain data structures that exist only on the computer system and not a component remote from the multiprocessor computer. For these reasons, claims 50 and 60 are, therefore, not anticipated by Intel.

Amended claims 70 and 76 are directed towards a computer-readable medium containing instructions causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer. Intel fails to disclose executing instructions causing a computer system to use processor compatibility information to select a new processor. As was discussed above, Intel discloses data structures that are required for compliance with the MultiProcessor specification and does not teach a method of selecting a new processor because it does not teach or fairly suggest executing a program or program instructions of any kind.

Moreover, amended claims 70 and 76 require obtaining processor compatibility information from a location that is remote from the multiprocessor computer. As was discussed

above, Intel discloses certain data structures. It does not teach or suggest a method for accessing these data structures or retrieving the information therein. Intel does not teach or suggest storing "compatibility information." Intel does teach storing certain types of information about processors in data structures, but it does not suggest or teach that this information is necessarily related to "compatibility." Even if it does suggest or teach storing "compatibility information," it does not disclose storing such information in a remote component. Instead, Intel discloses certain data structures that exist only on the computer system and not a component remote from the multiprocessor computer. Even if Intel does suggest a method for accessing these data structures, it is clear that these data structures exist only on the computer system and not on a computer that is remote from the multiprocessor computer. For these reasons, amended claims 70 and 76 are not anticipated by Intel.

Turning now to the Ghori reference, Claims 32 and 40 are not anticipated by Ghori because Ghori fails to disclose or suggest that the accessed processor compatibility information be located on, and retrieved from, a computer that is remote from the multiprocessor computer. In fact, Ghori teaches that CPU information be stored in the interprocessor circuitry or burned into the CPU itself. Claims 32 and 40 are, therefore, not anticipated by Ghori.

Amended claims 50 and 60 are directed towards a system for selecting a new processor for addition to a multiprocessor computer. Both claims require a "component remote from the multiprocessor computer that store processor compatibility information." To the degree that Ghori suggests storing "compatibility information," it does not disclose storing such information in a remote component. Instead, Ghori discloses storing CPU information in either a discrete memory device incorporated into the interprocessor circuitry or a ROM burned directly into the processor. Amended claims 50 and 60 are, therefore, not anticipated by Ghori.

Amended claims 70 and 76 are directed towards a computer-readable medium containing instructions causing a computer system to use processor compatibility information to select a new processor for addition to a multiprocessor computer. Amended claims 70 and 76 require obtaining processor compatibility information from a location that is remote from the multiprocessor computer. To the degree that Ghori suggests obtaining "compatibility information," it does not disclose obtaining such information in a remote component. Instead, Ghori discloses first storing CPU information in either a discrete memory device incorporated

into the interprocessor circuitry or a ROM burned directly into the processor, and then, accessing the stored information from one of these locations. Amended claims 50 and 60 are, therefore, not anticipated by Ghori.

Turning now to the Examiner's rejection of claims 36, 45, 57 and 67 under 35 U.S.C. § 103(a) based on Intel and in further view of Official Notice, Applicants respectfully disagree with the Examiner's grounds for taking Official Notice. Official Notice should only be taken by an examiner where the facts asserted to be well-known are capable of instant and unquestionable demonstration as being well-known. Here, the Examiner contends that although Intel does not expressly teach that "AP computers are connected to the BSP computer" via the Internet, such a practice was old and well known at the time of invention. First, it should be noted that the AP and the BSP(s) are *processors* and not "computers." With that being understood, although connecting computers together via the Internet may have been well-known at the time of invention, connection of individual processors via the Internet is not something that is capable of instant and unquestionable demonstration as being well-known at that time. On this basis, Applicants respectfully request that the rejection be withdrawn.

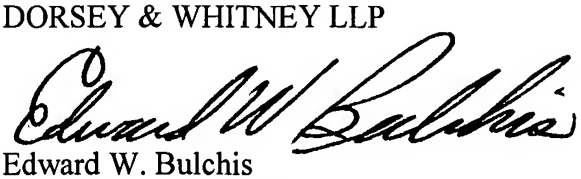
Even if the Examiner believes that the Official Notice is appropriate in this case, these claims are patentable over Official Notice based on the patentability of claims from which each depends.

The remaining claims in the application rejected over Intel and Ghori are patently distinguished over these references because of their dependency on patentable independent claims and because of additional limitations added by those claims.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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Enclosures:
Postcard
Fee Transmittal Sheet (+copy)
Copy of reference "Open VMS DCL Dictionary", pgs. 5-10

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